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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/578,511	05/26/2000	Won Hyoung Park	HI-004	7993
34610	7590	08/12/2004	EXAMINER	
FLESHNER & KIM, LLP			GHULAMALI, QUTBUDDIN	
P.O. BOX 221200			ART UNIT	
CHANTILLY, VA 20153			PAPER NUMBER	

2637

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

49

Office Action Summary

Application No.

09/578,511

Applicant(s)

PARK, WON HYOUNG

Examiner

Qutub Ghulamali

Art Unit

2631

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 March 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-42 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 6-20 is/are allowed.
- 6) ☒ Claim(s) 1,21-23,25-29,31-33,35-39,41 and 42 is/are rejected.
- 7) ☒ Claim(s) 2-5,24,30,34 and 40 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Acknowledgment

1. This Office Action is responsive to the Amendment filed on 03/12/2004.

Response to Arguments

2. In view of the Appeal Brief filed on March 12, 2004, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

- (1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,
- (2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 22, 23, 25-29, 31-33, 35-39, 41, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chalmers (US Patent 5,640,416).

Chalmers (figs. 3, 4, 5a), discloses an Analog-to-Digital converter (406) convert an intermediate frequency signal (214, 416) (aliased spectrum, see note below) into digital (digitized) signal (col. 4, lines 60-67), the digitized output from the A/D converter separates (308) and provides an In-phase (310) component and a quadrature (312) component of the digital signal (col. 7, lines 41-64), a plurality of filters (304,501) to filter the digital components in a polyphse low pass filter, outputs a complex corrected signal (col. 18, lines 45-59) using Code Division Multiple Access (CDMA) techniques. Chalmers fails to disclose providing a quadrature and an in-phase component of the digital signal. However, Chalmers shows at the output of the A/D converter the digitized signal separates (308) and provides an In-phase (310) component and a quadrature (312) component of the digital signal (col. 7, lines 41-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the separated digital components (first and second digital signals) outputted at the A/D converter device in such a way (in a single chip) so as to provide similarity of function (I and Q complex signal separation) as taught by Chalmers.

NOTE: By definition cited in "Technical Terms" second Edition by Daniel N. Lapedes, the alaising is an "Introduction of error into the computed amplitudes of the lower frequencies in a Fourier analysis of a function carried out using discrete time samplings

Art Unit: 2631

whose interval does not allow the proper analysis of the higher frequencies present in the analyzed function”.

5. Claim 21, is rejected under 35 U.S.C. 103(a) as being unpatentable over Efstathiou (US Patent No. 6,504,867).

Efstathiou discloses (figs. 1, 2) a wideband digital radio receiver (10), which receives an analog signal and provides two channels of digitized signal (29) (fig. 2), the channel separation shown (40, 42), provides an in-phase (I) and a quadrature (Q) signal (44, 46), with phase controlled by a numerically controlled oscillator (49), an analog IF signal adapted to provide a CDMA formatted signal as desired (col. 3, lines 33-64), a QPSK modulated digital signal (fig. 4) (col. 4, lines 22-44, 57-67), the matched filters include a first one-half in-phase component (matched FIR filter) and a second one-half quadrature component (matched FIR filter), an input circuit to amplify (16) a filtered (11) CDMA formatted input signal and provides an intermediate frequency (24) based on amplified input signal and a second signal processor (36,37) to output first and second digital signals on first and second channels (figs. 2, 4) and an output circuit to output signal having first and second Finite Impulse Response (FIR) filters to receive and filter the first and second digital signals, respectively (Figure 4). What Efstathiou does not disclose implicitly is a channel separator separate the first and second digital signals. Efstathiou, however, discloses providing two channels of digitized signal (29) (fig. 2), showing channel separation (40, 42), provide an in-phase (I) and a quadrature (Q) signal (44, 46). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the A/D digitized signal separated as first and second digital

Art Unit: 2631

signals elements (44, 46) (fig. 2) (40, 42) in such a way (in a single chip) so as to provide similarity of function (channel separation) as taught by Efstathiou.

Allowable Subject Matter/Reasons For Allowance

6. Claims 6-9, 10-20, allowed
7. Claims 2-5 and 24, 30, 34, 40, are objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.
8. The following is a statement of reasons for the indication of allowable subject matter:

The prior art does not teach or explicitly show; a digital sampler to sample the intermediate frequency (IF) signal, a zero-order hold device to determine an amplitude of the IF signal, a quantizer to convert the sampled IF signal processed by the zero-order hold device, a plurality of latches to transmit the digital signal from the quantizer to a plurality of channels after a prescribed time delay, and a plurality of output formatters to periodically output the latched digital signal transmitted to corresponding channels of the plurality of channels. Such limitations as recited in claim 6 is neither anticipated nor rendered obvious by the prior art of record.

Similarly, the prior art does not teach or fairly suggest; a plurality of negators to negate the latched digital signal and output a latched signal, and a plurality of selectors coupled to each of the plurality of negators to select and output one of the negated latched signal and a unprocessed latched digital signal. Such limitations as recited in claim 7 is neither anticipated nor rendered obvious by the prior art of record.

Art Unit: 2631

Similarly, the prior art does not teach or fairly suggest the plurality of output formatters comprise first and second output formatters, and wherein the output of each output formatters is received by a low pass filter. Such limitations, as recited in claims 8, are neither anticipated nor rendered obvious by the prior art of record.

Similarly, the prior art does not teach or fairly suggest the plurality of channels comprise an In-phase channel and a Quadrature channel. Such limitations, as recited in claims 9, are neither anticipated nor rendered obvious by the prior art of record.

Regarding claim 10, the prior art does not teach or explicitly show; a signal processor, comprising: a digitizer, which receives an analog signal and generates a digital signal, wherein the digitizer comprises: a sampler, which receives and samples the analog signal, a zero order hold circuit, which receives an output of the sampler and determines an amplitude of the received signal, and a quantizer, which receives an output of the zero order hold circuit and generates the digital signal, a channel separator, which receives the digital signal from the digitizer and separates the digital signal into at least 2 channels, each channel having a different phase; and a phase shift controller, which receives a clock signal and controls the phase shifting of the channel separator.

Such limitations as recited in claim 10 is neither anticipated nor rendered obvious by the prior art of record.

Similarly, dependent claims 11-20, recite limitations that are neither anticipated nor rendered obvious by the prior art of record.

NOTE: By definition cited in "Technical Terms" second Edition by Daniel N. Lapedes, the alaising is an "Introduction of error into the computed amplitudes of the lower

Art Unit: 2631

frequencies in a Fourier analysis of a function carried out using discrete time samplings whose interval does not allow the proper analysis of the higher frequencies present in the analyzed function”.

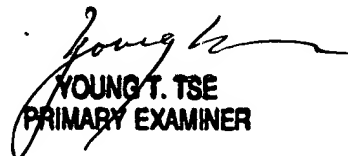
Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (703) 305-7868. The examiner can normally be reached on Monday-Friday from 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 703 308-7728. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QG.
August 4, 2004.


YOUNG T. TSE
PRIMARY EXAMINER